AMENDMENTS TO THE SPECIFICATION

a. Please replace the section titled **BRIEF DESCRIPTION OF THE DRAWINGS** with the following:

The invention may best be understood by reference to the following description taken in conjunction with the accompanying drawings, in which:

FIG. 1A depicts a perspective view of an exemplary cross point memory array employing a single layer of memory;

FIG. 1B depicts a perspective view of an exemplary stacked cross point memory array employing four layer of memory;

FIG. 1C depicts a cross section of a two layer stacked cross point array positioned over circuitry;

FIG. 2A depicts a plan view of selection of a memory cell in the cross point array depicted in FIG. 1A;

FIG. 2B depicts a perspective view of the boundaries of the selected memory cell depicted in FIG. 2A;

FIG. 2C depicts a cross section of the memory cell depicted in FIG. 2A;

FIG. 2D depicts a cross section of a portion of the memory cell depicted in FIG. 2A;

FIG. 3 depicts a generalized representation of a memory cell that can be used in a transistor memory array; ~~and~~

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FIG. 4 depicts an exemplary flow chart of various processing steps that could be involved in fabrication of a memory;

FIG. 5 depicts a detailed cross section of a memory cell in a cross point memory array.

It is to be understood that, in the drawings, like reference numerals designate like structural elements. Also, it is understood that the depictions in the FIGs. are not necessarily to scale.

b. Please add the following new paragraphs after paragraph **[0019]**:

[0019.1] FIG. 1C depicts a cross-section of an exemplary high-density NVRAM 120 having two memory layer in a stacked cross point array configuration. The high-density NVRAM 120 is preferably made up an array portion 122 and a memory circuit portion 124. The memory circuit portion 124 contains all of the active devices (devices that require a source of energy for their operation, such as transistors and amplifiers) needed to operate the high-density NVRAM 120. Those skilled in the art will recognize that standard fabrication techniques (e.g., CMOS processing) can be used to manufacture the memory circuit portion 124.

[0019.2] The array portion 122 includes a first layer of x-direction conductive array lines (X_0 layer) 126, a second layer of x-direction conductive array lines (X_1 layer) 128, a layer of y-direction conductive array lines (Y_0 layer) 130, a first memory plug layer (ML_0) 132 situated between the X_0 layer 126 and the Y_0 layer 130, a second memory plug layer (ML_1) 134 situated between the Y_0 layer 130 and the X_1 layer 128, a first plurality of X_0 thrus 136 and a first plurality of X_1 thrus 138. A plurality of vias 140 and metallization layers 142 together provide conductive paths from components of the memory circuit portion 124 to memory cells of the array portion 122. Similarly, the thrus 136 and 138 provide conductive paths from memory cells of the array portion 122 to the memory circuit portion 124. It should be noted that the thrus of the array portion 122 must be conductive and, therefore, will have different electrical properties that the memory layers at the same height.

c. Please add the following new paragraphs after paragraph **[0022]**:

[0022.1] FIG. 2C depicts a side view of an exemplary five-layer memory plug 255 with a non-ohmic device. The five layers are: a first electrode layer 260, a layer of a multi-resistive state element 265, a second electrode layer 270, a layer making up the non-ohmic device 275, and a third electrode 280. Some layers may actually be made up of multiple thin films. For example, one type of non-ohmic device 275 uses a three film metal-insulator-metal (MIM) structure. Additionally, certain multi-resistive state elements use multiple thin films (see FIG. 2D). Furthermore, not all the layers are required for every memory plug 255 or 310 (see FIG. 3) configuration. For example, certain cross point arrays may use means other than the non-ohmic device 275 to prevent unselected memory plugs from being disturbed.

[0022.2] In an alternative embodiment, at least one additional interface can be created within the multi-resistive state element by adding an additional conductive metal oxide layer.

[0022.3] The additional conductive metal oxide layer need not comprise the same material, however, interfaces between conductive metal oxide layers are difficult areas to control. As can be appreciated by one skilled in the art, mismatched lattices, possible inter-atom diffusion mechanisms, and adhesion issues are all relevant. Therefore, using substantially similar materials is one way to avoid such control issues.

[0022.4] Including dopants in only a portion of the conductive metal oxide, or using different dopants in adjacent portions allows the use of substantially similar materials for the conductive metal oxide layers, thus avoiding the control issues while imparting enough differences between the substantially similar materials to constitute and create an active

interface. Additionally, dopants may impart additional benefits, such as enhancing the memory effect of the memory element by creating traps.

[0022.5] Thus, for example, in one aspect of the present invention, FIG. 2D depicts a cross sectional view of an exemplary memory plug 310. In this example, a conductive metal oxide layer 290 that includes a metal oxide strontium zirconate doped with chromium is sandwiched between two substantially similar conductive metal oxide layers 285 and 295. The top conductive metal oxide layer is strontium zirconate doped with iron, which results in a p-type metal oxide layer 285. The bottom conductive metal oxide layer is strontium zirconate doped with niobium, which results in an n-type metal oxide layer 295.

[0022.6] In similar fashion, one skilled in the art can appreciate that only two layers of conductive metal oxides may be utilized without departing from the scope of the present invention.

[0022.7] As another example of the present invention, it is also possible to use different materials to form the conductive metal oxide layers, as long as these materials are compatible.

d. Please add the following new paragraph after paragraph **[0037]**:

[0037.01] FIG. 5 is a detailed cross section of a memory cell 500 in a cross point array using processing steps described in FIG. 4. A barrier/adhesion layer 1010 of 100Å of Ti followed by 200Å of TiN could be sputtered on the wafer, followed by 5000Å of W deposited using CVD, followed by etchback or CMP to remove W on the ILD surface 1002, leaving W plugs 1005 in the contact holes.

[0037.02] Once the plugs are formed, the W conductive array lines 1020 are patterned. Since W has a relatively high resistivity, the maximum length and minimum cross-sectional area may be limited in

comparison to aluminum or copper. Specifically, the maximum length and cross-sectional area of the conductive array lines 1020 can be determined using $R = \rho L/A$ and setting a maximum resistance to about 10kΩ in order to maintain fast access times. Assuming 5000Å thick metallization layers and a feature size of 0.25μm, the length of the conductive array lines 1020 would be a maximum of about 2000μm long. The W conductive array lines 1020 can be achieved through a barrier/adhesion layer 1015 of 100Å of Ti plus 200Å of TiN, followed by 5000Å of W deposition through CVD, followed by mask, etch, and resist strip steps.

[0037.03] Another ILD layer 1025 could be deposited over the first layer of conductive array lines 1020. The dielectric layer 1025 can be a thick layer of SiO_2, deposited over the W conductive array lines 1020 by plasma-enhanced chemical vapor deposition (PECVD) and then planarized by CMP to expose the top surfaces of the W lines 1020.

[0037.04] The bottom electrodes 1030 are then deposited. First, a 500Å thick barrier layer of TiN or TiAlN is deposited to prevent metal inter-diffusion, followed by a 200Å conductive oxide layer of $LaNiO_3$ (LNO) or $SrRuO_3$ (SRO). These layers can be deposited by sputtering. Alternatively to the conductive oxide layer a 500 Å layer of Ir can be deposited, followed by a 200 Å layer of IrO_2. These layers can be deposited by reactive sputtering from an Ir target, adding oxygen in the sputtering chamber to create the IrO_2 layer.

[0037.05] Then, approximately 2000Å of multi-resistive state element 1035 having a stoichiometry of $Pr_{0.7}Ca_{0.3}MnO_3$ is deposited at about 600°C by a physical vapor deposition technique such as sputtering. As previously explained, the multi-resistive state element 1035 would have a low resistance of 100k Ohm and a high resistance of 1M Ohm, and would change state with a less than 50ns flat pulse at 2V. Another electrode 1040 (200Å of LNO or SRO and another 500Å of TiN are deposited via sputtering) is deposited on top of the multi-resistive state element 1035.

[0037.06] The optional non-ohmic device 1045 can be formed by first sputtering 250Å of Pt or Al, followed by 50Å or less of Al_2O_3, and another 250Å of sputtered Pt or Al. The Al_2O_3 could be formed by atomic layer deposition (ALD) or oxidization of Al. The Al_2O_3 thickness would be chosen to achieve a V_{NO+} of 4V. After the optional non-ohmic device 1045, another 500Å barrier layer 1050 of sputtered TiN is optionally deposited to prevent metal inter-diffusion.

[0037.07] Then, standard photolithography and appropriate multi-step etch processes could be used to pattern the memory/non-ohmic film stack into memory cell plugs. The spaces between the plugs could then be filled in by depositing a 250Å etch stop/diffusion barrier 1055 of Si_3N_4, followed by a thick SiO_2 interlayer dielectric (ILD) 1060, which is planarized by CMP.

[0037.08] An etch stop layer is used to ensure a thin-film does not get removed during processing. When etching a thin-film layer, the actual etch time is normally longer than that minimum time required to etch through the film. This overetch time, typically 20-50% of the minimum etch time, is added to allow for variations in film thickness and variations in etch rate due to pattern density. An etch stop layer, with an etch rate significantly lower than that of the film being etched, can be used to protect the layers beneath it from attack during the overetch time. The etch stop layer can later be removed or etched through in selected locations by using a different etch method (e.g. different chemistry) producing a high etch rate for the etch stop layer and a lower etch rate compared to underlying layers.

[0037.09] The diffusion barrier layer 1055 additionally protects the memory plugs from inter-diffusion with the surrounding dielectric1060. Regardless of whether such an insulating barrier 1055 is necessary for the entire plug, or only certain components, it is often useful to coat the entire plug with the diffusion barrier layer 1055 for simplicity.

[0037.10] Although not shown in FIG. 5, via holes with W plugs could be formed to contact the tops of the memory cell islands and are one mechanism that can be used to provide connections between metal interconnect layers. Standard photolithography and a 2-step via etch (stopping first on the Si_3N_4 layer 1055, then etching through it) could be used to expose the tops of the memory cell islands. These via holes could be filled by depositing 100Å of Ti, followed by 200Å of TiN, followed by a 5000Å W layer. CMP could then be used to remove W on the ILD surface1060, leaving the W plugs in the via holes.

[0037.11] If there are no more memory elements to form at high temperature, the final layer of conductive array lines may comprise aluminum, copper or other high conductivity metal. A top layer of conductive array lines could then be formed by depositing, in order, another barrier/adhesion layer 1065 of 100Å of Ti and 200Å of TiN, then the conductive array line 1070 comprising 5000Å of an Al/Cu mixture, and then a final barrier/adhesion layer 1075 of 100Å of Ti, 200Å of TiN. An anti-reflective coating (ARC) 1080, such as SiON could also be deposited. A final mask, etch and resist strip would then be performed. The final cross-point memory array could then be 16384 W conductive array lines by 4096 Al/Cu conductive array lines to create a 64Mbit array. 16 of these arrays could be laid side-by-side to create a 1Gbit memory.

Appendix: Marked up paragraphs showing changes from applications incorporated by reference.

a. Paragraphs 114 – 115 from 10/360,005, filed February 7, 2003, and published as 20040160819 on August 19, 2004.

~~Figure 4B~~ FIG. 1C depicts a cross-section of ~~a bit block 402 of~~ an exemplary high-density NVRAM ~~400~~ 120 having two memory layer in a stacked cross point array configuration. The high-density NVRAM ~~400~~ 120 is preferably made up an array portion ~~405~~ 122 and a memory circuit portion ~~410~~ 124. The memory circuit portion ~~410~~ 124 contains all of the active devices (devices that require a source of energy for their operation, such as transistors and amplifiers) needed to operate the high-density NVRAM ~~400~~ 120. ~~The circuitry of the memory circuit portion 410 will be described in connection with Figure 6 and those~~ Those skilled in the art will recognize that standard fabrication techniques (e.g., CMOS processing) can be used to manufacture the memory circuit portion ~~410~~ 124.

The array portion ~~405~~ 122 includes a first layer of x-direction conductive array lines (X_0 layer) ~~415~~ 126, a second layer of x-direction conductive array lines (X_1 layer) ~~420~~ 128, a layer of y-direction conductive array lines (Y_0 layer) ~~425~~ 130, a first memory plug layer (ML_0) ~~430~~ 132 situated between the X_0 layer ~~415~~ 126 and the Y_0 layer ~~425~~ 130, a second memory plug layer (ML_1) ~~435~~ 134 situated between the Y_0 layer ~~425~~ 130 and the X_1 layer ~~420~~ 128, a first plurality of X_0 thrus ~~440~~ 136 and a first plurality of X_1 thrus ~~445~~ 138. A plurality of vias ~~450~~ 140 and metallization layers ~~455~~ 142 together provide conductive paths from components of the memory circuit portion ~~410~~ 124 to memory cells of the array portion ~~405~~ 122. Similarly, the thrus ~~440~~ 136 and ~~445~~ 138 provide conductive paths from memory cells of the array portion ~~405~~ 122 to the memory circuit portion 124. It should be noted that the thrus of the array portion ~~405~~ 122 must be conductive and, therefore, will have different electrical properties that the memory layers at the same height.

b. Paragraph 42 from 10/605,757 filed October 23, 2003, and published as 20040159867 on August 19, 2004.

FIG. [[7]] 2C depicts a side view of an exemplary five-layer memory plug ~~305~~ 255 with a non-ohmic device. The five layers are: a first electrode layer ~~705~~ 260, a layer of a multi-resistive

state element ~~710~~ 265, a second electrode layer ~~715~~ 270, a layer making up the non-ohmic device ~~720~~ 275, and a third electrode ~~725~~ 280. Some layers may actually be made up of multiple thin films. For example, one type of non-ohmic device ~~720~~ 275 uses a three film metal-insulator-metal (MIM) structure. Additionally, certain multi-resistive state elements use multiple thin films (see FIG. 2D). Furthermore, not all the layers are required for every memory plug ~~305~~ 255 or ~~610~~ 310 (see FIG. 3) configuration. For example, certain cross point arrays may use means other than the non-ohmic device ~~720~~ 275 to prevent unselected memory plugs from being disturbed. **[remainder of paragraph not used]**

c. Paragraphs 84 – 87 from 10/605,757 filed October 23, 2003, and published as 20040159867 on August 19, 2004.

In an alternative embodiment, ~~a structure where the memory effect can be located independently of the interface between the electrode and the memory material is disclosed. For example,~~ at least one additional interface can be created within the multi-resistive state element by adding an additional conductive metal oxide layer.

The additional conductive metal oxide layer need not comprise the same material, however, interfaces between conductive metal oxide layers are difficult areas to control. As can be appreciated by one skilled in the art, mismatched lattices, possible inter-atom diffusion mechanisms, and adhesion issues are all relevant. Therefore, using substantially similar materials is one way to avoid such control issues.

Including dopants in only a portion of the conductive metal oxide, or using different dopants in adjacent portions allows the use of substantially similar materials for the conductive metal oxide layers, thus avoiding the control issues while imparting enough differences between the substantially similar materials to constitute and create an active interface. Additionally, dopants may impart additional benefits, such as enhancing the memory effect of the memory element by creating traps.

Thus, for example, in one aspect of the present invention, FIG. [[9]] 2D depicts a cross sectional view of an exemplary memory plug ~~900~~ 310. In this example, a ~~A~~ conductive metal oxide layer ~~910~~ 290 that includes a metal oxide strontium zirconate doped with chromium is sandwiched between two substantially similar conductive metal oxide layers ~~905~~ 285 and ~~915~~ 295. The top conductive metal oxide layer is strontium zirconate doped with iron, which results

in a p-type metal oxide layer ~~905~~ 285. The bottom conductive metal oxide layer is strontium zirconate doped with niobium, which results in an n-type metal oxide layer ~~915~~ 295. *[Remainder of paragraph not used]*

d. Paragraph 93 from 10/605,757 filed October 23, 2003, and published as 20040159867 on August 19, 2004.

In similar fashion, one skilled in the art can appreciate that only two layers of conductive metal oxides may be utilized without departing from the scope of the present invention. *[Remainder of paragraph not used]*

e. Paragraph 94 from 10/605,757 filed October 23, 2003, and published as 20040159867 on August 19, 2004.

As another example of the present invention, it is also possible to use different materials to form the conductive metal oxide layers, as long as these materials are compatible. *[Remainder of paragraph not used]*

f. Paragraph 74 – 86 from 10/682,277 filed October 8, 2003, and published as 20040159868 on August 19, 2004.

FIG. 5 is a detailed cross section of a memory cell 500 in a cross point array using processing steps described in FIG. 4. A barrier/adhesion layer 1010 of 100Å of Ti followed by 200Å of TiN could be sputtered on the wafer, followed by 5000Å of W deposited using CVD, followed by etchback or CMP to remove W on the ILD surface 1002, leaving W plugs 1005 in the contact holes.

Once the plugs are formed, the W conductive array lines 1020 are patterned ~~on the wafer at 920~~. Since W has a relatively high resistivity, the maximum length and minimum cross-sectional area may be limited in comparison to aluminum or copper. Specifically, the maximum length and cross-sectional area of the conductive array lines 1020 can be determined using $R = \rho L/A$ and setting a maximum resistance to about 10kΩ in order to maintain fast access times. Assuming 5000Å thick metallization layers and a feature size of 0.25μm, the length of the conductive array lines 1020 would be a maximum of about 2000μm long. The W conductive array lines 1020 can be achieved through a barrier/adhesion layer 1015 of 100Å of Ti plus 200Å

of TiN, followed by 5000Å of W deposition through CVD, followed by mask, etch, and resist strip steps.

Another ILD layer 1025 could be deposited over the first layer of conductive array lines **1020** ~~at 925~~. The dielectric layer 1025 can be a thick layer of SiO_2, deposited over the W conductive array lines 1020 by plasma-enhanced chemical vapor deposition (PECVD) and then planarized by CMP to expose the top surfaces of the W lines 1020.

~~At step 930 the~~ **The** bottom electrodes 1030 are **then** deposited. First, a 500Å thick barrier layer of TiN or TiAlN is deposited to prevent metal inter-diffusion, followed by a 200Å conductive oxide layer of $LaNiO_3$ (LNO) or $SrRuO_3$ (SRO). These layers can be deposited by sputtering. Alternatively to the conductive oxide layer a 500 Å layer of Ir can be deposited, followed by a 200 Å layer of IrO_2. These layers can be deposited by reactive sputtering from an Ir target, adding oxygen in the sputtering chamber to create the IrO_2 layer.

~~At step 935~~ **Then,** approximately 2000Å of multi-resistive state element 1035 having a stoichiometry of $Pr_{0.7}Ca_{0.3}MnO_3$ is deposited at about 600°C by a physical vapor deposition technique such as sputtering. As previously explained, the multi-resistive state element 1035 would have a low resistance of 100k Ohm and a high resistance of 1M Ohm, and would change state with a less than 50ns flat pulse at 2V. ~~At 940 another~~ **Another** electrode 1040 (200Å of LNO or SRO and another 500Å of TiN are deposited via sputtering) is deposited on top of the multi-resistive state element 1035.

~~At 945 through 955 the optional non-ohmic device 1045 is formed.~~ The **optional non-ohmic** device 1045 can be formed by first sputtering 250Å of Pt or Al, followed by 50Å or less of Al_2O_3, and another 250Å of sputtered Pt or Al. The Al_2O_3 could be formed by atomic layer deposition (ALD) or oxidization of Al. The Al_2O_3 thickness would be chosen to achieve a V_{NO+} of 4V. After the optional non-ohmic device 1045, another 500Å barrier layer 1050 of sputtered TiN is optionally deposited ~~in step 955~~ to prevent metal inter-diffusion.

~~At 960~~ **Then,** standard photolithography and appropriate multi-step etch processes could be used to pattern the memory/non-ohmic film stack into memory cell plugs. ~~At 965 the~~ **The** spaces between the plugs could then be filled in by depositing a 250Å etch stop/diffusion barrier 1055 of Si_3N_4, followed by a thick SiO_2 interlayer dielectric (ILD) 1060, which is planarized by CMP.

An etch stop layer is used to ensure a thin-film does not get removed during processing. When etching a thin-film layer, the actual etch time is normally longer than that minimum time required to etch through the film. This overetch time, typically 20-50% of the minimum etch time, is added to allow for variations in film thickness and variations in etch rate due to pattern density. An etch stop layer, with an etch rate significantly lower than that of the film being etched, can be used to protect the layers beneath it from attack during the overetch time. The etch stop layer can later be removed or etched through in selected locations by using a different etch method (e.g. different chemistry) producing a high etch rate for the etch stop layer and a lower etch rate compared to underlying layers.

The diffusion barrier layer 1055 additionally protects the memory plugs from inter-diffusion with the surrounding dielectric1060. Regardless of whether such an insulating barrier 1055 is necessary for the entire plug, or only certain components, it is often useful to coat the entire plug with the diffusion barrier layer 1055 for simplicity.

~~At 970 via holes are formed (not shown in FIG. 10).~~ Although not shown in FIG. 5, via ~~Via~~ holes with W plugs could be formed to contact the tops of the memory cell islands and are one mechanism that can be used to provide connections between metal interconnect layers. Standard photolithography and a 2-step via etch (stopping first on the Si_3N_4 layer 1055, then etching through it) could be used to expose the tops of the memory cell islands. These via holes could be filled by depositing 100Å of Ti, followed by 200Å of TiN, followed by a 5000Å W layer. CMP could then be used to remove W on the ILD surface1060, leaving the W plugs in the via holes.

If there are no more memory elements to form at high temperature, the final layer of conductive array lines may comprise aluminum, copper or other high conductivity metal. A top layer of conductive array lines could then be formed ~~at 980~~ by depositing, in order, another barrier/adhesion layer 1065 of 100Å of Ti and 200Å of TiN, then the conductive array line 1070 comprising 5000Å of an Al/Cu mixture, and then a final barrier/adhesion layer 1075 of 100Å of Ti, 200Å of TiN. An anti-reflective coating (ARC) 1080, such as SiON could also be deposited. A final mask, etch and resist strip would then be performed. The final cross-point memory array could then be 16384 W conductive array lines by 4096 Al/Cu conductive array lines to create a 64Mbit array. 16 of these arrays could be laid side-by-side to create a 1Gbit memory.